Req :
Pour répondre aux questions du sujet, seules les pages 1/36, 20 à 24/36 sont nécessaires

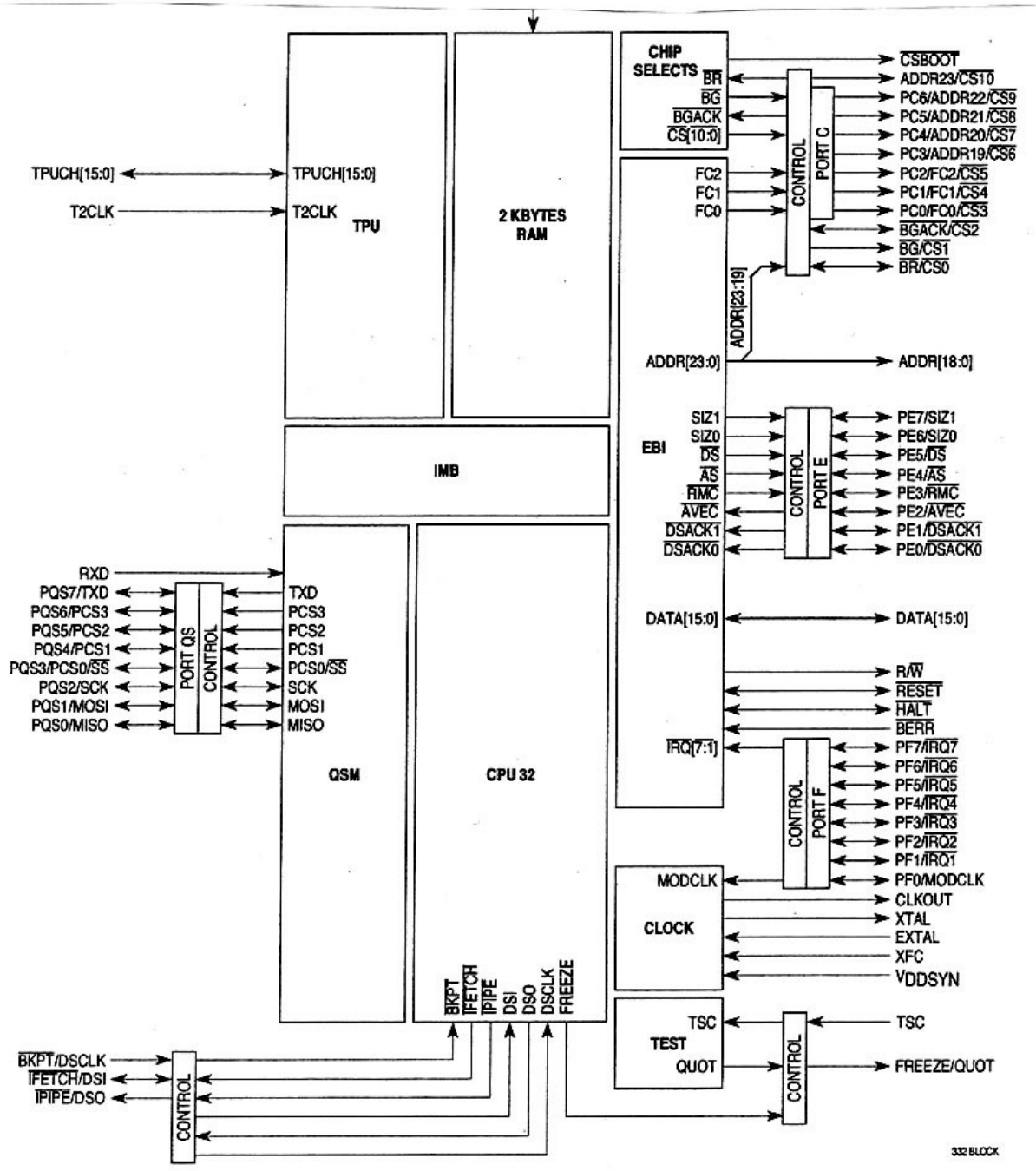

Figure 3-1 MCU Block Diagram

7.9.3 $\overline{\text{CSBOOT}}$ Base Address and Option Registers

The $\overline{\text{CSBOOT}}$ assignment field in CSPAR0 is configured differently from the other pin assignment fields. The MSB (bit 1) of the $\overline{\text{CSBOOT}}$ assignment field in CSPAR0, has a reset value of one. This enables the $\overline{\text{CSBOOT}}$ signal to select a boot ROM containing initialization firmware. The LSB value, determined by the logic level of DATA0 during reset, selects boot ROM port size. When DATA0 is held low, port size is 8 bits. When DATA0 is held high (either by the weak internal pull-up driver or by an external pull-up device), port size is 16 bits.

After reset, the MCU fetches initialization vectors beginning at word address $000000. To support bootstrap operation from reset, the base address field in chip-select base address register boot (CSBARBT) has a reset value of all zeros. A ROM device containing a reset vector beginning at its base address can be enabled by $\overline{\text{CSBOOT}}$ after a reset.

Table 7-8 shows the reset values in the base and option registers for $\overline{\text{CSBOOT}}$.

Table 7-8 $\overline{\text{CSBOOT}}$ Base and Option Register Reset Values

Field	Reset Value
Base Address	$000000
Block Size	1 Mbyte*
Timing Mode	Emulates Asynchronous Bus Cycles
Upper/Lower Byte	Both Bytes
Read/Write	Read/Write
Strobe ($\overline{\text{AS}}$/$\overline{\text{DS}}$)	$\overline{\text{AS}}$
$\overline{\text{DSACK}}$	13 Wait States
Address Space	Supervisor/User Space
IPL	Any Level
Autovector	Interrupt Vector Externally

*Default block size is effectively 512 Kbyte on CPU16-based MCUs since values of ADDR[23:20] follow ADDR19.

7.10 Chip-Select Register Diagrams

Chip-select registers include two pin assignment registers, two base address registers, twelve option registers, and a discrete output data register.

7.10.1 Chip-Select Pin Assignment Registers

The pin assignment registers contain 12 two-bit fields ($\overline{\text{CS}}$[10:0] and $\overline{\text{CSBOOT}}$) that determine the functions of the chip-select pins. Each pin has two or three possible functions, as shown below. Pins that have no discrete output function do not use the %00 encoding.

Bit Field	Description
00	Discrete Output
01	Alternate Function
10	Chip Select (8-Bit Port)
11	Chip Select (16-Bit Port)

NOTE

On MCUs with a reduced pin-count SIM, some chip-select pins may not be available. Refer to the user's manual for the particular MCU for details.

Pin assignments at reset are determined by the states of the data bus pins indicated in the following register diagrams. Refer to **7.9 Chip-Select Reset Operation** for additional information on pin assignments at reset.

CSPAR0 — Chip-Select Pin Assignment Register 0 **$####44**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	CSPA0[6]		CSPA0[5]		CSPA0[4]		CSPA0[3]		CSPA0[2]		CSPA0[1]		$\overline{\text{CSBOOT}}$	
RESET:															
0	0	DATA2	1	DATA2	1	DATA2	1	DATA1	1	DATA1	1	DATA1	1	1	DATA0

CSPAR0 contains seven two-bit fields that determine the functions of corresponding chip-select pins. CSPAR0[15:14] are not used. These bits always read zero; writes have no effect. CSPAR0 bit 1 always reads one; writes to CSPAR0 bit 1 have no effect.

Table 7-9 CSPAR0 Pin Assignments

CSPAR0 Field	Chip Select Signal	Alternate Signal	Discrete Output
CSPA0[6]	$\overline{\text{CS5}}$	FC2	PC2
CSPA0[5]	$\overline{\text{CS4}}$	FC1	PC1
CSPA0[4]	$\overline{\text{CS3}}$	FC0	PC0
CSPA0[3]	$\overline{\text{CS2}}$	$\overline{\text{BGACK}}$	—
CSPA0[2]	$\overline{\text{CS1}}$	$\overline{\text{BG}}$	—
CSPA0[1]	$\overline{\text{CS0}}$	$\overline{\text{BR}}$	—
$\overline{\text{CSBOOT}}$	$\overline{\text{CSBOOT}}$	—	—

CSPAR1 — Chip-Select Pin Assignment Register 1 **$####46**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	CSPA1[4]		CSPA1[3]		CSPA1[2]		CSPA1[1]		CSPA1[0]	
RESET:															
0	0	0	0	0	0	DATA7	1	DATA6	1	DATA5	1	DATA4	1	DATA3	1

CSPAR1contains five two-bit fields that determine the functions of corresponding chip-select pins. CSPAR1[15:10] are not used. These bits always read zero; writes have no effect.

Table 7-10 CSPAR1 Pin Assignments

CSPAR0 Field	Chip Select Signal	Alternate Signal	Discrete Output
CSPA1[4]	$\overline{\text{CS10}}$	ADDR23	ECLK
CSPA1[3]	$\overline{\text{CS9}}$	ADDR22	PC6
CSPA1[2]	$\overline{\text{CS8}}$	ADDR21	PC5
CSPA1[1]	$\overline{\text{CS7}}$	ADDR20	PC4
CSPA1[0]	$\overline{\text{CS6}}$	ADDR19	PC3

7.10.2 Chip-Select Base Address Registers

CSBARBT contains the base address for selection of a bootstrap peripheral memory device. Bit and field definition for CSBARBT and CSBAR[10:0] are the same, but reset block sizes differ. Refer to **7.2 Chip-Select Base Addresses** for more information.

CSBARBT — Chip-Select Base Address Register Boot ROM **$####48**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR 23	ADDR 22	ADDR 21	ADDR 20	ADDR 19	ADDR 18	ADDR 17	ADDR 16	ADDR 15	ADDR 14	ADDR 13	ADDR 12	ADDR 11	BLKSZ		
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

CSBAR[10:0] — Chip-Select Base Address Registers **$####4C–$####74**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR 23	ADDR 22	ADDR 21	ADDR 20	ADDR 19	ADDR 18	ADDR 17	ADDR 16	ADDR 15	ADDR 14	ADDR 13	ADDR 12	ADDR 11	BLKSZ		
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADDR[15:3] — Base Address Field
This field sets the starting address of a particular address space.

BLKSZ — Block Size Field
This field determines the size of the block above the base address that is enabled by the chip select.

7.10.3 Chip-Select Option Registers

Option register fields determine timing of and conditions for assertion of chip-select signals. CSORBT contains parameters that support bootstrap operations from peripheral memory devices. Bit and field definitions for CSORBT and CSOR[10:0] are the same, but their reset settings differ.

CSORBT — Chip Select Option Register Boot ROM **$####4A**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODE	BYTE		R/$\overline{W}$		STRB	$\overline{DSACK}$				SPACE		IPL			$\overline{AVEC}$
RESET:															
0	1	1	1	1	0	1	1	0	1	1	1	0	0	0	0

CSOR[10:0] — Chip Select Option Registers **$####4E–$####76**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODE	BYTE		R/$\overline{W}$		STRB	$\overline{DSACK}$				SPACE		IPL			$\overline{AVEC}$
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MODE — Timing Mode

The MODE bit determines whether chip-select operation emulates asynchronous bus operation or is synchronized to the M6800-type bus clock signal (ECLK) available on ADDR23. Refer to **7.5 Chip-Select Timing** for additional information.

0 = Emulate asynchronous bus operation
1 = Synchronize chip-select assertion to ECLK

BYTE — Upper/Lower Byte Option

This field enables or disables the chip-select circuit and, for 16-bit ports, determines which combinations of size and ADDR0 pins will cause the chip select to be asserted. Refer to **7.6 Chip Selects and Dynamic Bus Sizing** for more information.

00 = Disable
01 = Lower byte
10 = Upper byte
11 = Both Bytes

R/$\overline{W}$ — Read/Write

This field causes a chip select to be asserted only for a read, only for a write, or for both read and write.

00 = Reserved
01 = Read only
10 = Write only
11 = Read/Write

STRB — Address Strobe/Data Strobe

The STRB bit controls the timing of a chip-select assertion in asynchronous mode. This bit has no effect in synchronous mode.

0 = Synchronize chip select assertion with address strobe
1 = Synchronize chip select assertion with data strobe

$\overline{DSACK}$ — Data and Size Acknowledge

This field specifies the source of $\overline{DSACK}$ when chip-select cycles emulate asynchronous bus cycles, and controls wait state insertion. Refer to **7.6 Chip Selects and Dynamic Bus Sizing** for details.

SPACE — Address Space Select

The SPACE field determines the address space in which a chip select is asserted. An access must have the space type represented by SPACE encoding in order for a chip-select signal to be asserted. Refer to **7.8 Using Chip Selects in Interrupt Acknowledge Cycles** for additional information.

00 = CPU space
01 = User space
10 = Supervisor space
11 = Supervisor or user space

IPL — Interrupt Priority Level

This field selects the interrupt level when a chip select is used for interrupt acknowledge. Refer to **7.8 Using Chip Selects in Interrupt Acknowledge Cycles** for additional information.

000 = Any Level
001 = Level 1
010 = Level 2
011 = Level 3
100 = Level 4
101 = Level 5
110 = Level 6
111 = Level 7

$\overline{\text{AVEC}}$ — Autovector Enable

This field specifies whether to generate an internal $\overline{\text{AVEC}}$ signal during an interrupt acknowledge cycle initiated by assertion of an $\overline{\text{IRQ}}$ pin when match conditions are met. Refer to **7.8 Using Chip Selects in Interrupt Acknowledge Cycles** for additional information.

0 = Disable $\overline{\text{AVEC}}$ generation
1 = Enable $\overline{\text{AVEC}}$ generation

7.10.4 Port C Data Register (PORTC)

The port C data register latches data for pins programmed as discrete outputs. When a pin is assigned as a discrete output, the value in this register appears at the output. PC[6:0] correspond to CS[9:3]. This is a read/write register. Bit 7 is not used. Writing to this bit has no effect, and a read returns zero. Refer to **7.3 Pin Assignments and Discrete Output** for more information on this register.

PORTC — Port C Data Register **$####40**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED								0	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:								1	1	1	1	1	1	1	1