Hardware Manual

IPC@CHIP Embedded Controller Family
SC11/SC12/SC13

High Performance, 80186- and 80188-Compatible,
16-Bit Embedded Microcontroller
Single Chip PC with Flash, RAM, Watchdog

Non RoHS compliant		RoHS compliant	
Name	**Ordering Code**	**Name**	**Ordering Code**
SC11	538428	SC11-LF	543327
SC11-IEC	539384	SC11-IEC-LF	543328
SC12	20040112	SC12-LF	542490
SC12-F	537227	SC12-F-LF	542491
SC13	536079	SC13-LF	542546
SC13-F	538429	SC13-F-LF	542547
SC13-IEC	540553	SC13-IEC-LF	542752

Mature Products - Not recommended for new designs



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1. BASIC SPECIFICATIONS

@CHIP	CPU	RAM	FLASH	Ethernet
SC11	BECK 186 40MHz	512 Kbytes	512 Kbytes	-
SC12	AMD 186ED 20MHz	512 Kbytes	512 Kbytes	10Base-T
SC13	BECK 186 40MHz	512 Kbytes	512 Kbytes	10/100Base-T

IPC@CHIP® family 80186- and 80188-compatible microcontroller with up to 512KB RAM, 512KB Flash and Ethernet on Chip
- Lower system cost with higher performance

High performance
- up to 40MHz operating frequency
- 1 Mbyte internal memory space
- 6 x 256-byte I/O space
- Low-power CMOS process with single 5V power supply

Enhanced integrated peripherals
- Up to 14 programmable I/O (PIO) pins
- Two full-featured asynchronous serial ports allow full-duplex, 7-bit or 8-bit data transfers, Serial port hardware handshaking with CTS and RTS selectable for each port
  Independent serial port baud rate generators
  DMA to and from the serial ports
- Ethernet controller IEEE 802.3 10Base-T/100Base-TX[1]
  Autonegotiation : 10/100, Full/Half Duplex[2]
- Watchdog timer
- Pulse-width demodulation option

Familiar 80C186 peripherals
- Two independent DMA channels
- Programmable interrupt controller with up to six external interrupts
- Two programmable 16-bit timers, interrupt capable
- Programmable memory and peripheral chip-select logic

Software-compatible with the 80C186 and 80C188 microcontrollers with widely available native development tools, applications, and system software

Pre-installed Real Time Operating System (@CHIP RTOS)

Available in the following packages:
- 32-pin, plastic pack (DIL32)

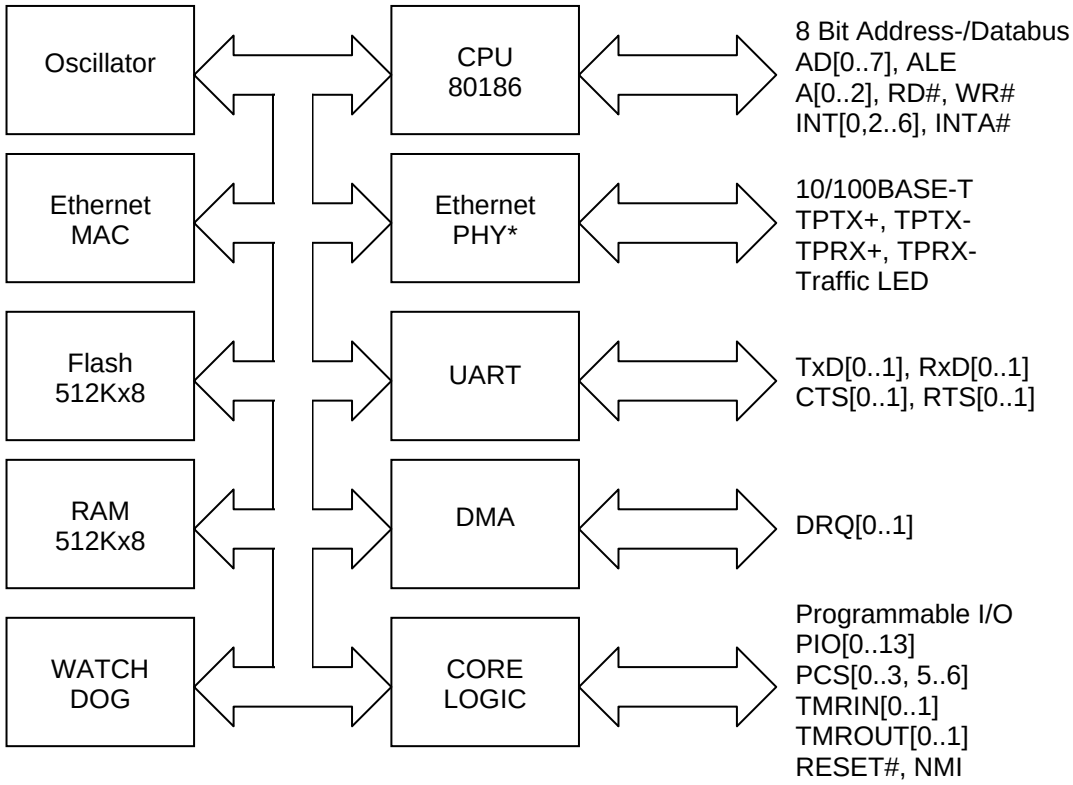
The extension '-LF' indicates, that the controller is a RoHS compliant component.

The Beck IPC@CHIP® family of System on Chip microcontrollers and microprocessors is based on the x86 architecture. The IPC@CHIP® family microcontroller is the ideal solution for new designs requiring Ethernet TCP/IP communication over twisted pair and/or through the serial port. The compatibility with the 80C186/188 family makes it also an ideal upgrade for systems based upon this processor range but requiring increased performance, serial communications, Ethernet communications, a direct bus interface, or more than 64K of memory.
The IPC@CHIP® family microcontrollers integrate up to 512Kbyte RAM with increased performance and up to 512Kbyte FLASH, reducing memory subsystem costs.
The minimum endurance of the Flash memory is 10,000 cycles (depending on environmental stress e.g. temperature).

[1] 10/100BASE-T only for SC13
[2] Autonegotiation only for SC13

The IPC@CHIP® family microcontrollers also integrate the functions of the CPU, multiplexed address bus, three timers, watchdog timer, chip selects, interrupt controller, two DMA controllers, two asynchronous serial ports, and programmable I/O (PIO) pins on one chip.
It also supports I²C-Bus and SPI (Serial Peripheral Interface) at any PIO pins via software emulation.
The IPC@CHIP® microcontroller is a highly integrated design that provides all Media Access Control (MAC) and Encode-Decode (ENDEC) functions in accordance with the IEEE 802.3 standard. Network interfaces including 10/100Base-T via the Twisted-pair. The integrated 10/100Base-T transceiver makes IPC@CHIP® more cost-effective.
Compared to the 80C186/188 microcontrollers, the IPC@CHIP® family microcontrollers
enable designers to reduce the size, power consumption, and cost of embedded systems, while increasing reliability, functionality and performance.
The IPC@CHIP® family microcontrollers have been designed to meet the most common requirements of embedded products developed for the communications, office automation, mass storage, and general embedded markets. Specific applications including industrial controls, data collection, protocol conversion, process monitoring and internet connectivity.

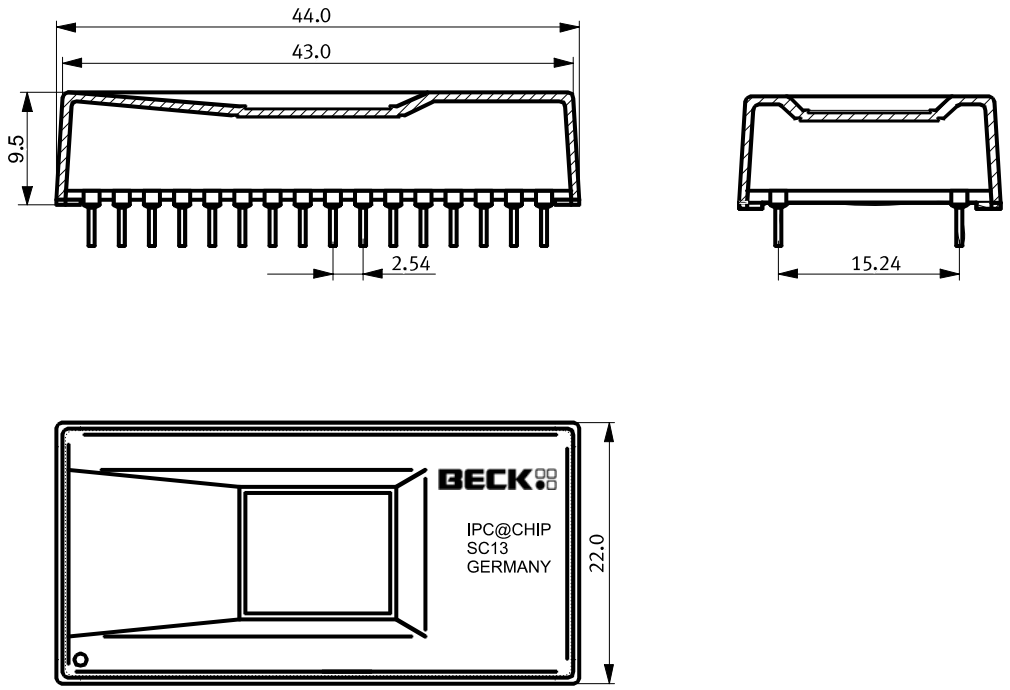
IPC@CHIP® family microcontroller block diagram



Picture 1.1: Access to hardware components via API functions.
* SC12 and SC13 only

2. PHYSICAL DIMENSIONS

The package is physically identical for SC11, SC12 and SC13.



Picture 2.1: IPC@CHIP physical dimensions

3. DESIGN AND HANDLING GUIDLINES

A DIL32 socket must be used within a wave soldering process or a reflow process.

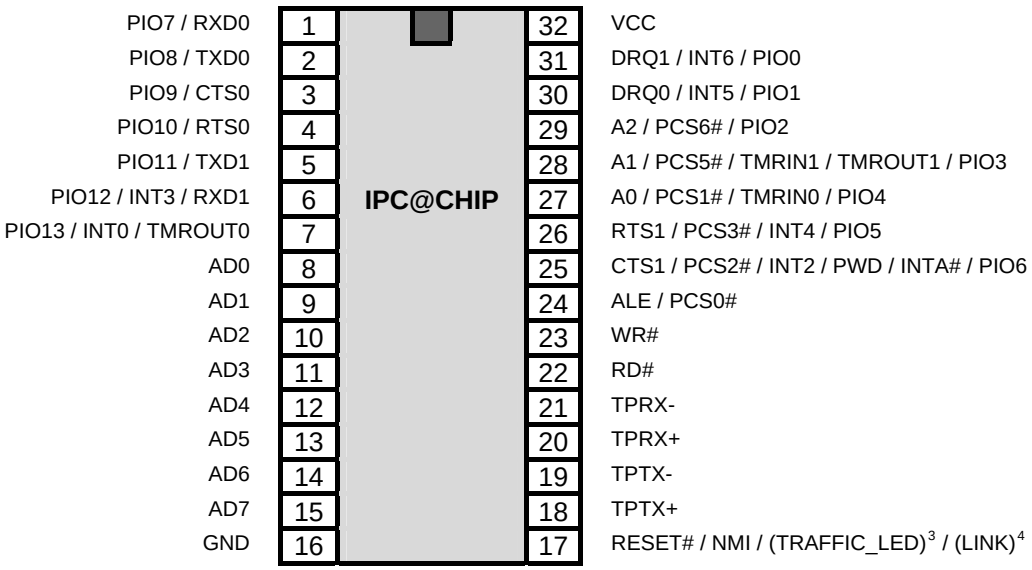
The SC1x should not be plugged into the socket during the soldering process.



Electrostatic Sensitive Device

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4. PIN CONFIGURATION



Picture 4.1: IPC@CHIP pin configuration

Note: Locate decoupling capacitors as close to VCC Pin as physically possible.

[3] Traffic only SC12 and SC13
[4] Link status only SC12

5. PIN FUNCTIONS

Pin Terminology
The following terms are used to describe the pins:
Input (I) - An input-only pin.
Input (IS) - An input-only pin with Schmitt Trigger.
Output (O) - An output-only pin.
Input/Output (I/O) - A pin that can be either input or output.

5.1 Address / Data bus

Pin Name	Type	Function
A[0..2]	O	**Address Bus (output, three-state)** These pins supply nonmultiplexed memory or I/O addresses to the system. During a bus hold or reset condition, the address bus is in a high-impedance state. A0–A2 will serve as the nonmultiplexed address bus for external peripherals. A0-A2 covers an address range of 8 Bytes max.
AD[0..7]	I/O	**Multiplexed Address and Data Bus (input/output, three-state, level-sensitive)** These time-multiplexed pins supply partial memory or I/O addresses, as well as data, to the system. This bus supplies the low-order 8 bits of an address to the system during the first period of a bus cycle (t1), and it supplies data to the system during the remaining periods of that cycle (t2 , t3 , and t4). In 8-bit mode, AD7–AD0 supplies the data for both high and low bytes. During a bus hold or reset condition, the address and data bus is in a high-impedance state.
ALE	O	**Address Latch Enable (output)** This pin indicates to the system that an address appears on the address and data bus (AD7–AD0). The address is guaranteed to be valid on the trailing edge of ALE. ALE is three-stated and held resistively Low during a bus hold condition. In addition, ALE has a weak internal pulldown resistor that is active during reset, when it is enabled by software.
RD#	O	**Read Strobe (output, three-state)** This pin indicates to the system that the microcontroller is performing a memory or I/O read cycle. RD is guaranteed to not be asserted before the address and data bus is floated during the address-to-data transition. RD floats during a bus hold condition.
WR#	O	**Write Strobe (output)** This pin indicates to the system that the data on the bus is to be written to a memory or I/O device. WR floats during a bus hold or reset condition.

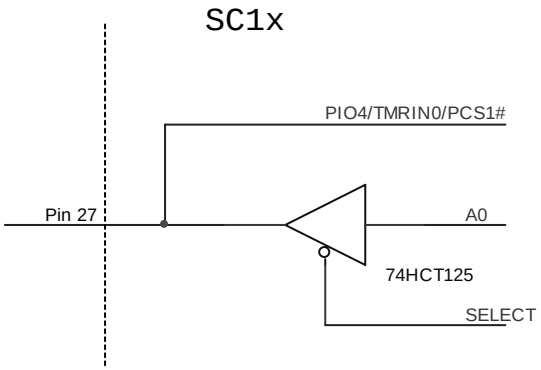
5.2 Programmable I/O Pins

Pin Name	Type	Function
PIO[0..13]	I/O	**Programmable I/O Pins (input/output, open-drain)** The IPC@CHIP® family microcontroller provides 14 individually programmable I/O pins. Each PIO can be programmed with the following attributes: PIO function (enabled/disabled), direction (input/output), and weak pullup or pulldown.

PIO#	After power-on reset, the PIO pin defaults to	Programmable as Input with
0	Input without	pullup
1	Input without	pullup
2	Input with pullup	pullup
3	Input with pullup	pullup / pulldown
4*	Input with pullup	pullup
5	Input with pullup	pullup
6	Input with pullup	pullup
7	RxD0	pullup
8	TxD0	pullup
9	Input with pullup	pullup
10	Input with pullup	pullup
11	TxD1	pullup
12	RxD1	pullup
13	Input with pulldown	pulldown

Internal Pullup and Pulldown is approximately 7-10kOhm.

*PIO4 can also be programmed as A0 through the RTOS. The following schematic shows the principle circuit inside the SC1x.

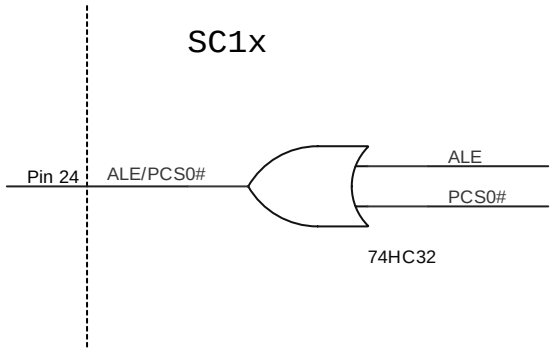


Picture 5.1: Principle insight of pin 27

5.3 Programmable Chip Selects

Pin Name	Type	Function
PCS[0..3]	O	**Peripheral Chip Selects (output)** These pins indicate to the system that an I/O memory access is in progress to the corresponding region of the peripheral memory. PCS0–PCS3 are three-stated and held resistively High during a bus hold condition. In addition, PCS0–PCS3 each have a weak internal pullup resistor that is active during reset. The PCS outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range.
PCS[5..6]	O	**Peripheral Chip Selects (output)** These pins indicate to the system that an I/O memory access is in progress to the corresponding region of the peripheral memory. PCS5–PCS6 are three-stated and held resistively High during a bus hold condition. In addition, PCS5–PCS6 each have a weak internal pullup resistor that is active during reset. The PCS outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range.

PCS0# can also be programmed as ALE through the RTOS. The following schematic shows the principle circuit inside the SC1x.



Picture 5.2: Principle insight of pin 24

5.4 Interrupts

Pin Name	Type	Function
INT[0,2-6]	I	**Maskable Interrupt Request (input)** These pins indicate to the microcontroller that an interrupt request has occurred. If the INT pin is not masked, the microcontroller transfers program execution to the location specified by the corresponding INT vector in the microcontroller interrupt vector table. Interrupt requests are synchronised internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT until the request is acknowledged. INT2 becomes INTA# when INT0 is configured in cascade mode.
INTA#	O	**Interrupt Acknowledge (output)** When the microcontroller interrupt control unit is operating in cascade mode, this pin indicates to the system that the microcontroller needs an interrupt type to process the interrupt request on INT0. The peripheral issuing the interrupt request must provide the microcontroller with the corresponding interrupt type.
PWD	IS	**Pulse Width Demodulator (input, Schmitt trigger)** If pulse width demodulation is enabled, PWD processes the signal through a Schmitt trigger. PWD is used internally to drive TMRIN0 and INT2, and PWD is inverted internally to drive TMRIN1 and INT4. If INT2 and INT4 are enabled and timer 0 and timer 1 are properly configured, the pulse width of the alternating PWD signal can be calculated by comparing the values in timer 0 and timer 1. In PWD mode, the signals TMRIN0, TMRIN1 and INT4 can be used as PIOs. If they are not used as PIOs, they are ignored internally.

5.5 Timer

Timer can be clocked internally or externally. Maximum frequency is ¼ CPU clock. If the timer will be clocked internally the timer out pin (TMROUT) may be used. External clock at Input and output at the same time with same timer is not possible.

Pin Name	Type	Function
TMRIN[0..1]	I	**Timer Input (input, edge-sensitive)** These pins supply a clock or control signal to the internal microcontroller timer 0 and 1. After internally synchronising a Low-to-High transition on TMRIN, the microcontroller increments the corresponding timer. TMRIN must be tied High if not being used. When PIO is enabled, TMRIN is pulled High internally. TMRIN0 is driven internally by INT2/PWD when pulse width demodulation mode is enabled. The TMRIN0 pin can be used as a PIO when pulse width demodulation mode is enabled.
TMROUT[0..1]	O	**Timer Output (output)** These pins supply the system with either a single pulse or a continuous waveform with a programmable duty cycle.

5.6 10/100Base-T Interface

Pin Name	Type	Function
TPTX[+,-]	O	**Twisted Pair Driver (outputs)**
TPRX[+,-]	I	**Twisted Pair Receive (inputs).**
TRAFFIC LED (LINK LED)[5]	O	**Traffic LED Driver (output)** This pin indicates network traffic by sinking voltage to 3V. It is generated through an open-collector low mode for a short impulse to indicate the presence of traffic on the network. Note that this pin is not able to source any current!

[5] Link status only SC12

5.7 Asynchronous Serial Ports

All asynchronous port pins are TTL level. To provide RS232 or RS485 level external drivers must be connected (like MAX232). The following modes can be provided:
Full-Duplex Operation with 7-bit or 8-bit, odd, even or no parity. Error detection is possible with parity errors, framing errors, overrun errors and break character recognition. Hardware handshaking (Clear-to-send CTS and Request-to-send RTS) is possible.
To get a definite baud rate, a baud rate divider must be provided. A general formula for the baud rate divisor is: BAUDDIV = (CPU clock / (16 x Baud Rate)). We recommend to using the RTOS function "Get Frequencies".
The maximum baud rate is achieved by setting BAUDDIV=0001h. This results in a baud rate of 1250Kbit for SC12 and 2500 Kbit for SC11/SC13. A BAUDDIV setting of zero results in no transmission or reception of data.
The serial port receiver tolerance depends on the used settings:

SC11/SC13	SC12
9 Bits ± 3.47% 10 Bits ± 3.125% 11 Bits ± 2.84%	+ 3.0% - 2.5%

The two ports can operate at different rates.

Pin Name	Type	Function
TxD[0..1]	O	**Transmit Data (output)** These pins supply asynchronous serial transmit data to the system from serial port 0 and 1.
RxD[0..1]	I	**Receive Data (input)** These pins supply asynchronous serial receive data from the system to asynchronous serial ports 0 and 1.
CTS[0..1]	I	**Clear-to-Send (input)** These pins provide the Clear-to-Send signal for asynchronous serial port 0 and 1 when hardware flow control is enabled for the port. The CTS signals gate the transmission of data from the associated serial port transmit register. When CTS is asserted, the transmitter begins transmission of a frame of data, if any is available. If CTS is deasserted, the transmitter holds the data in the serial port transmit register. The value of CTS is checked only at the beginning of the transmission of the frame.
RTS[0..1]	O	**Request-to-Send 0 (output)** These pins provide the Request-to-Send signal for asynchronous serial ports 0 and 1 when hardware flow control is enabled for the port. The RTS signals are asserted when the associated serial port transmit register contains data that has not been transmitted.

5.8 DMA

Pin Name	Type	Function
DRQ[0..1]	I	**DMA Request (input, level-sensitive)** These pins indicate to the microcontroller that an external device is ready for DMA channel 0 or 1 to perform a transfer. DRQ is level-triggered and internally synchronised. DRQ is not latched and must remain active until serviced.

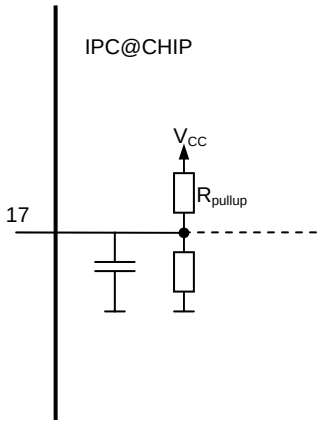
5.9 Reset, Power Fail Generator

Note that RESET# pin shares 3(4) functions: RESET and NMI as described here, as well as network traffic (and link status for SC12) as described in the corresponding chapters.
This is a voltage-multiplexed pin that internally sinks current in the case of a ethernet packet send/receive. All peripheral logic asserted to this pin must be open-collector to prevent the internal logic from sinking too high current. The pin is already provided with an internal pullup resistor.

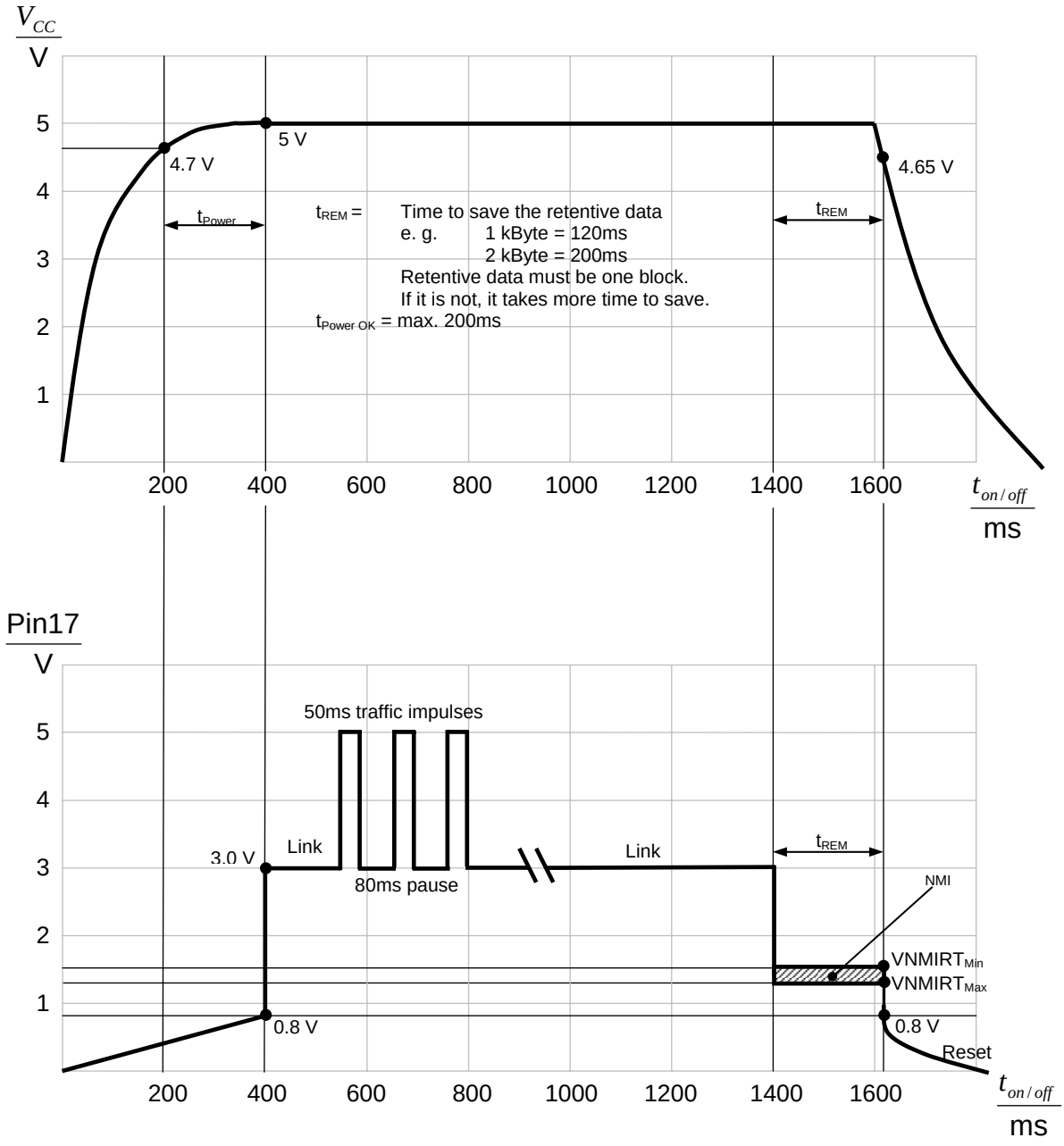
	R_{pullup}
SC11	4.7 kOhm
SC12	1 kOhm
SC13	4.7 kOhm

Pin Name	Type	Function
RESET#	I	**Reset (input/level-sensitive)** If voltage on this pin goes below 0.8V the microcontroller will perform a reset. In that case the microcontroller immediately terminates its present activity, clears its internal logic, and transfers CPU control to the reset address.
NMI	I	**Nonmaskable Interrupt (input, level-sensitive)** If voltage on this pin goes down below VNMIRT (see DC CHARACTERISTICS) it indicates to the microcontroller that an interrupt request has occurred. The NMI signal is the highest priority hardware interrupt and, unlike the INT6–INT0 pins, cannot be masked. The microcontroller always transfers program execution to the location specified by the nonmaskable interrupt vector in the microcontroller interrupt vector table when NMI is asserted. The NMI is for detecting low supply power and the following data backup only. A reset has to follow after the NMI. To guarantee that the interrupt is recognised, the NMI condition must be asserted to the pin until reset.

The following schematic delivers a principle insight of pin 17.



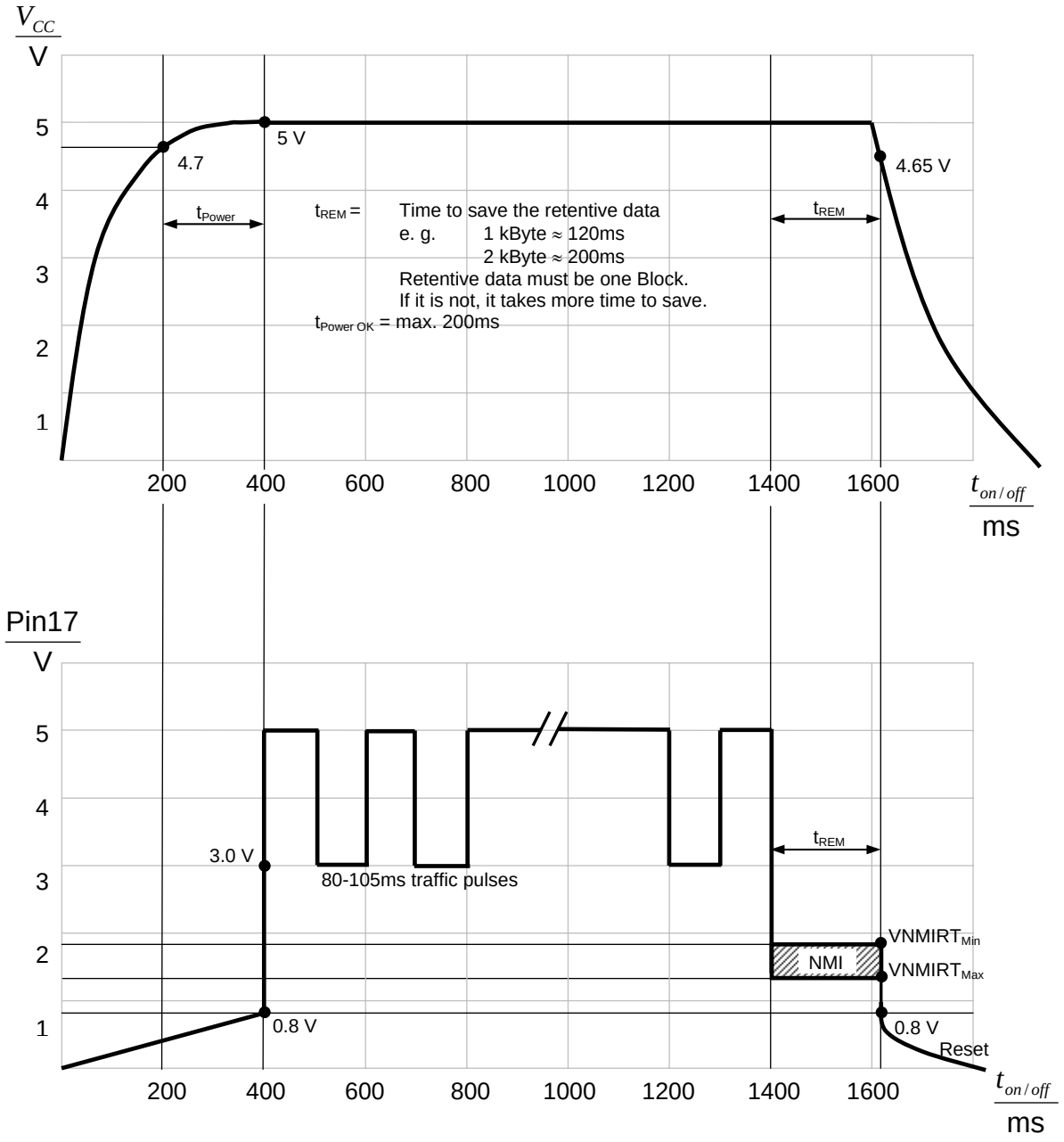
5.10 NMI reset traffic LED sequence SC12



To implement time to save the retentive data keep Pin 17 at VNMIRT[6] and VCC at 5V for t_{REM} with external capacitors. If Pin 17 goes below 0.8V IPC@CHIP will be in reset state.
Grafic applies to a configuration, where a LED is connected from Pin 17 to V_{CC} over a resistor.

[6] see DC-Characteristics

5.11 NMI reset traffic LED sequence SC13



To implement time to save the retentive data keep Pin 17 at VNMIRT[7] and VCC at 5V for t_{REM} with external capacitors. If Pin 17 goes below 0.8V IPC@CHIP will be in reset state.
Grafic applies to a configuration, where a LED is connected from Pin 17 to V_{CC} over a resistor.

[7] see DC Characteristics

5.12 Startup Pin configuration

At turn-on the IPC@Chip I/O pins are configured as follows:

Pin1: RXD0/PIO7 = RXD0
Pin2: TXD0/PIO8 = TXD0
Pin3: CTS0/PIO9 = Input pullup
Pin4: RTS0/PIO10 = Input pullup
Pin5: TXD1/PIO11 = TXD1
Pin6: RXD1/PIO12 = RXD1
Pin7: TMROUT0/INT0/PIO13 = Input pulldown
Pin17: RESET/NMI/TRAFFIC = Input
Pin24: ALE/PCS0 = Output, value 1
Pin25: CTS1/PCS2/PIO6/INT2 = Input pullup
Pin26: RTS1/PCS3/PIO5/INT4 = Input pullup
Pin27: PCS1/PIO4/TMRIN0/A0 = Input pullup
Pin28: PCS5/PIO3/TMROUT1/TMRIN1/A1 = Input pullup
Pin29: PCS6/PIO2/A2 = Input pullup
Pin30: INT5/PIO1 = Input
Pin31: INT6/PIO0 = Input

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6. MUTUALLY EXCLUSIVE FUNCTIONS

The IPC@CHIP® family microcontroller provides a lot of different functions by several multi-function pins. Choosing one function will result in disabling other functions. The following table shows, which functions are mutually exclusive.

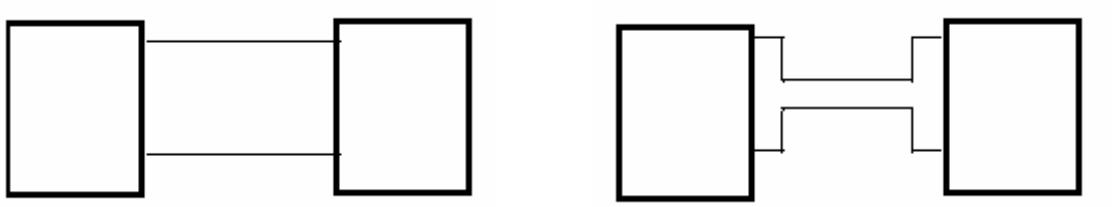
Pin Name	Function	Exclusion
A0	nonmultiplexed address A0	PIO4, PCS1#, TMRIN0
A[1..2]	nonmultiplexed address A[1..2]	PIO[2..3], PCS[5..6], Timer 1
ALE	Address / Data bus	PCS0#
CTS0	hardware flow control Serial Port 0	PIO9
CTS1	hardware flow control Serial Port 1	PIO6, PCS2#, INT2, INTA#, PWD
DRQ0	DMA Request 0	PIO1, INT5
DRQ1	DMA Request 1	PIO0, INT6
INT0	Interrupt Request 0	PIO13, TMROUT0, cascaded Interrupt Controller
INT2	Interrupt Request 2	PIO6, PCS2#, INTA#, PWD, hardware flow control Serial Port 1
INT3	Interrupt Request 3	PIO12, Serial Port 1
INT4	Interrupt Request 4	PIO5, PCS3#, SPI, hardware flow control Serial Port 1
INT5	Interrupt Request 5	PIO1, DRQ0
INT6	Interrupt Request 6	PIO0, DRQ1
INTA#	cascaded Interrupt Controller	PIO6, PIO13, INT0, INT2, PCS2#, PWD, TMROUT0, HW flow control Serial Port 1
PWD	Pulse Width Demodulator	PIO6, PCS2, INT2, INT4, TMROUT[0..1], TMRIN[0..1], INTA#, cascaded Interrupt Controller, HW flow control Serial Port 1
PCS0#	programmable chip select 0	Address/Data bus
PCS1#	programmable chip select 1	A0, PIO4, TMRIN0
PCS2#	programmable chip select 2	PIO6, INT2, INTA#, PWD, HW flow control Serial Port 1, cascaded Interrupt Controller
PCS3#	programmable chip select 3	PIO5, INT4, hardware flow control Serial Port 1
PCS5#	programmable chip select 5	A[1..2], PIO3, Timer 1
PCS6#	programmable chip select 6	A[1..2], PIO2
PIO0	Programmable I/O	DRQ1, INT6
PIO1	Programmable I/O	DRQ0, INT5
PIO2	Programmable I/O	A2, PCS6#
PIO3	Programmable I/O	A1, PCS5#, Timer 1
PIO4	Programmable I/O	A0, PCS1#, TMRIN0
PIO5	Programmable I/O	PCS3#, INT4, hardware flow control Serial Port 1
PIO6	Programmable I/O	PCS2#, INT2, cascaded Interrupt Controller, PWD, HW flow control Serial Port 1
PIO7	Programmable I/O	Serial Port 0
PIO8	Programmable I/O	Serial Port 0
PIO9	Programmable I/O	Hardware flow control Serial Port 0
PIO10	Programmable I/O	Hardware flow control Serial Port 0
PIO11	Programmable I/O	Serial Port 1
PIO12	Programmable I/O	Serial Port 1, INT3
PIO13	Programmable I/O	INT0, cascaded Interrupt Controller, TMROUT0
RxD0, TxD0	Serial Port 0 w/o HW flow control	PIO[7..8]
RxD0, TxD0 CTS0, RTS0	Serial Port 0 with HW flow control	PIO[7..10]
RxD1, TxD1	Serial Port 1 w/o HW flow control	PIO[11..12], INT3
RxD1, TxD1 CTS1, RTS1	Serial Port 1 with HW flow control	PIO[5..6,11..12], INT3, PCS[2..3]#, INT2, INT4, PWD, cascaded Interrupt Controller

7. ETHERNET 10/100BASE-T

7.1 10Base-T Media Filter Placement and Termination for SC12

Placement of the termination components TPTX+ and TPTX- should be located as physically close to the media filter as possible.

The media filter should also placed as physically close to the RJ-45 connector as possible to minimise stray EMI transfer to the media. The trace routing is to keep the area enclosed by a circuit loop as small as possible to minimise the incidence of magnetic coupling. However this can conflict with the general rule of keeping trace lengths to a minimum. For example, if circuit components are positions along the same sides of a square, the best return is back along the same three sides of the square, NOT directly back along the fourths side. This rule must be strictly adhered to. Furthermore, there should never be an unnecessary feed-through inside the circuit loop. This also implies that the circuit loop should never encircle the power/ground planes (i.e. part of the circuit loop above and part of circuit loop below these planes).



Incorrect Layout Correct Layout

The two traces of the pair should always be routed in adjacent channels and should be of same length. To reduce capacitive coupling, each circuit loop should be separated from the others. Circuit loops can be separated either by physical space (if located on the same layer) or by placement of signal layers on the opposite side of the power/ground planes. The following signal groups should be isolated from each other. Width of receiver trace should be 25 mil minimum to achieve 50Ohm impedance characteristic at 10MHz. Width of transmitter trace should be 10 mil minimum to achieve 25Ohm impedance characteristic at 10MHz
To achieve optimum performance the designer must protect the magnetics from the environment. It should be isolated from the power and ground planes.

7.2 Magnetics approved for use for 10Base-T application

Through-Hole PCB:

BEL FUSE, Inc. part no. 0556-5999-19		(http://www.belfuse.com)
Halo Electronics, Inc.	Part no. FS22-101Y4	(http://www.haloelectronics.com)
BECK-IPC GmbH	Part no. FS22-101Y4	(online shop ordering number 20003276)
Valor, Inc. part no. FL1012/1066		(http://www.valorinc.com/)

Surface-Mount PCB:

Valor, Inc. part no. SF1012	(http://www.valorinc.com/)

7.3 Routing and placement rules for SC13 and Ethernet components

1. Place the RJ45 connector, the magnetics and the SC13 as close together as possible.
2. If No. 1 is not possible, keep the RJ45 and the magnetics as close as possible. This will allow remote placement of the SC13.
3. Select and place the magnetics as the best routing scheme from the SC13 to the magnetics to the RJ45 connector.
4. Place the 49.9Ω TX termination pull-ups (TPTX+/TPTX-, pin 18/19) as close to the magnetics as possible.
5. Place the two 24.9Ω RX series resistors as close to the magnetics as possible.
6. Place the two 24.9Ω RX termination resistors and the 10 nF capacitor (TPRX+, pin 20 & TPRX-, pin 21) as close to the SC13 as possible.
7. Place the 75Ω cable side center tap termination resistors and the 1nF capacitor as close to the magnetics as possible.
8. Place the Unused Wire Pair termination resistors and the 1nF capacitor as close to the RJ45 connector as possible.
9. The traces connecting the transmit outputs (TPTX+, pin 18) & (TPTX-, pin 19) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
10. The traces connecting the transmit outputs from the magnetics to pins 1 & 2 on the RJ45 connector must be run as differential pairs. The differential impedance should be 100 ohms.
11. The traces connecting the receive inputs (TPRX+, pin 20) & (TPRX-, pin 21) from the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.
12. The traces connecting the receive inputs on the magnetics from pins 3 & 6 on the RJ45 connector must be run as differential pairs. The differential impedance should be 100 ohms.
13. Typically, all planes are cleared out from under the differential pairs connecting the RJ45 and the magnetics. The plane clear out boundary is usually halfway through the magnetics.
14. Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, etc.). The electrical engineer needs to work with the PCB designer to determine all these variables.
15. Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the IPC@CHIP). Any noise from other traces may couple into the Ethernet section and cause problems.

7.4 Suggested Magnetics

Surface-Mount PCB:

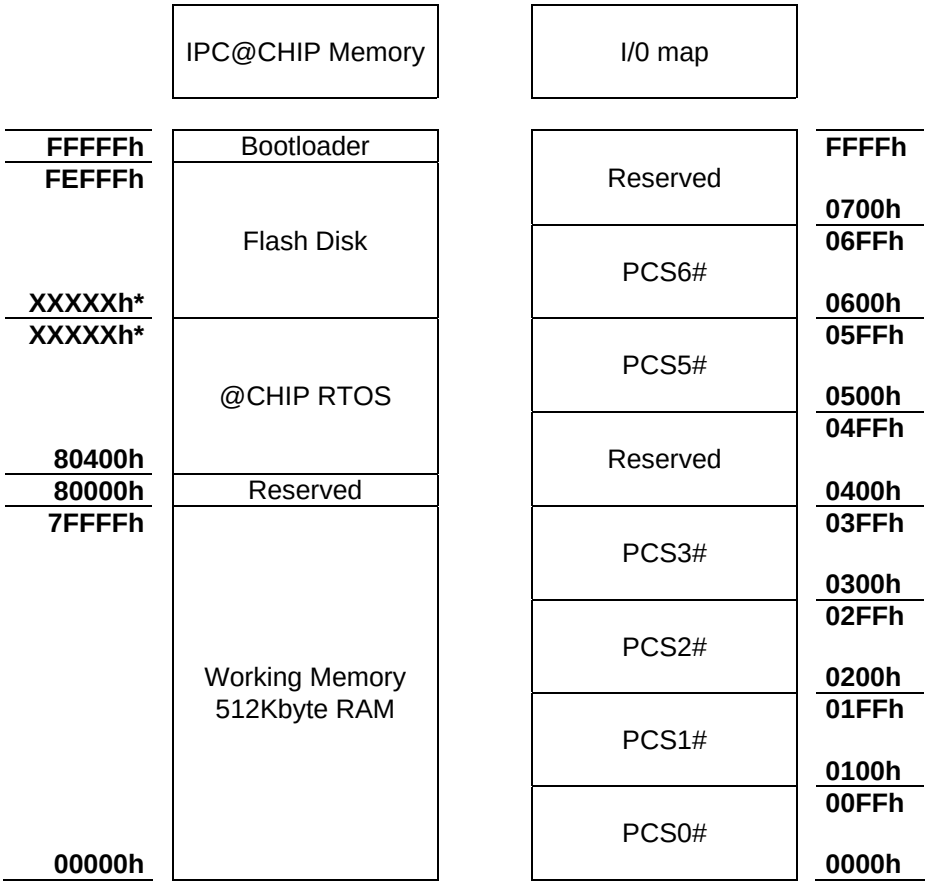
BECK-IPC GmbH	Part no. Magnetic FS23	(online shop ordering number: 538431)
Halo Electronics, Inc.	Part no.TG110-S050N2	(http://www.haloelectronics.com)
BECK-IPC GmbH	Part no. Magnetic FM24	(online shop ordering number: 556366)
UMEC Europe	Part no. LU1S041-34-LF	(http://www.umeu.de/)
TAIMAG	Part no. RJSL-003TC1	(http://www.taimag.com/)

Through-Hole PCB:

BECK-IPC GmbH	Part no. Magnetic Module FM23	(online shop ordering number: 538430)

8. SYSTEM OVERVIEW

8.1 Memory map



picture 8.1: IPC@CHIP memory map

***** depends on the CHIP-RTOS version, see “Scaled @Chip-RTOS versions” in @CHIP-RTOS API Documentation

8.2 System interrupts

Source	Sensitivity
INT0 (external)	Edge / Level
Network controller (internal)	
INT2 (external)	Edge / Level
INT3 (external)	Edge / Level
INT4 (external)	Edge / Level
INT5 (external) / DMA Interrupt Channel 0 (if DMA is used)	Edge
INT6 (external) / DMA Interrupt Channel 1 (if DMA is used)	Edge
Reserved	
Timer0 (internal)	
Timer1 (internal)	
Timer 1ms (internal) (*)	
Serial port 0 (internal) (*)	
Serial port 1 (internal) (*)	
NMI (internal/external)	

(*) Internal used by @CHIP-RTOS, not available for user interrupt service functions

When an interrupt occurs all interrupts are disabled until the interrupts are released by setting IF Flag in the interrupt service routine. Interrupts of the same source are masked until the corresponding Bit in interrupt service register is cleared.
Level sensitive interrupts are triggered by a high level, edge sensitive interrupts by the rising edge.

8.3 Watchdog

The IPC@CHIP provides a true watchdog timer function. The watchdog can be used to regain control of the system when software fails to respond as expected. The watchdog is active after reset. The watchdog timeout period is about 838 ms. The mode can set to trigger the watchdog by the user program or by the CHIP-RTOS (default). In CHIP-RTOS mode, the CHIP-RTOS performs the watchdog strobing provided that the system's timer interrupt is allowed to execute. Beware that excessive interrupt masking periods can lead to system resets.

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9. CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS

	SC11(-LF) [2]	SC12(-LF) [2]	SC13(-LF) [2]
Storage temperature	-25°C to +100°C[1]	-25°C to +100°C[1]	-25°C to +100°C[1]
Supply voltage (V_{CC})	-0.3V to +6.0V	-0.3V to +6.0V	-0.3V to +6.0V
Supply current (V_{CC} = 5.25V)	240mA	220 mA	400 mA
Voltage on any pin with respect to ground	-0.3V to V_{CC} + 0.3V	-0.3V to V_{CC} + 0.3V	-0.3V to V_{CC} + 0.3V

[1]Note: Temperatures apply not for packing of SC1x.
[2]Note: Parameters applies for -LF and non-LF parts.

9.2 OPERATING RANGES

	SC11	SC12	SC13
Operating temperature (Ambient T_A)	0°C to +70°C	0°C to +70°C	0°C to +70°C
Supply voltage (V_{CC})	5.0V +/- 5%	5.0V +/- 5%	5.0V +/- 5%
Typical power supply current (at V_{CC})	180mA	180mA	300mA

	SC11-LF	SC13-LF
Operating temperature (Ambient T_A)	-25°C to +70°C [3]	-25°C to +70°C [3]
Supply voltage (V_{CC})	5.0V +/- 5%	5.0V +/- 5%
Typical power supply current (at V_{CC})	180mA	300mA

[3]Note: Operating Temperature were changed from 0°C to +70°C to -25°C to +70°C since delivery date 15.03.2006

Note: Exposure to conditions beyond those listed here may adversely affect the lifetime and reliability of the device.

9.3 DC CHARACTERISTICS

→ The following characteristics are also valid for lead free (-LF) and -F (without housing) products.

(Under operating ranges unless otherwise noted)

9.3.1 SC12 DC Characteristics

Symbol	Parameter Description	Test Condition	MIN.	TYP.	MAX.	Unit
I_{CC}	Current into V_{CC}			180	220	mA
VOL	Voltage Output Low	IOL = 2.0mA	-		0.45	V
VOH	Voltage Output High	IOH = -2.4mA	2.4		-	V
VILO	Voltage Input Low	-	-		0.8	V
VIHI	Voltage Input High	-	2.0		-	V
VRT	Reset Threshold		4.5	4.65	4.75	V
	Reset Threshold Hysteresis			0.04		V
VRESLO	IN Voltage Reset active		0		0.8	V
VRESOL	OUT Voltage Reset Low	IOL = -9mA			0.8	V
VNMIRT	NMI Threshold	VCC = 5V	1.3		1.5	V
Clout	External Load on AD[0..7], RD#, WR#				20	PF
	External Load on the other pins				30	PF
Clin	Input Capacitance				30	PF
RPIO	Internal Pullup/-down Resistor			10K		Ω

9.3.2 SC13/SC11 DC Characteristics

Symbol	Parameter Description	Test Condition	MIN.	TYP.	MAX.	Unit
I_{CC}	Current into V_{CC}	SC11		180	220	mA
I_{CC}	Current into V_{CC}	SC13		300	400	mA
VOL	Voltage Output Low	IOL = 4.0mA	-		1.5	V
VOH	Voltage Output High	IOH = -4.0mA	3.5		-	V
VILO	Voltage Input Low	-	-		1.5	V
VIHI	Voltage Input High	-	3.5		-	V
VRT	Reset Threshold		4.5	4.65	4.75	V
	Reset Threshold Hysteresis			0.04		V
VRESLO	IN Voltage Reset active		0		0.8	V
VRESOL	OUT Voltage Reset Low	IOL = -4mA			0.8	V
VNMIRT	NMI Threshold	VCC = 5V	1.3		1.8	V
Clout	External Load on AD[0..7], RD#, WR#				20	PF
	External Load on the other pins				30	PF
Clin	Input Capacitance				30	PF
RPIO	Internal Pullup/-down Resistor		7K		10K	Ω

9.4 AC CHARACTERISTICS

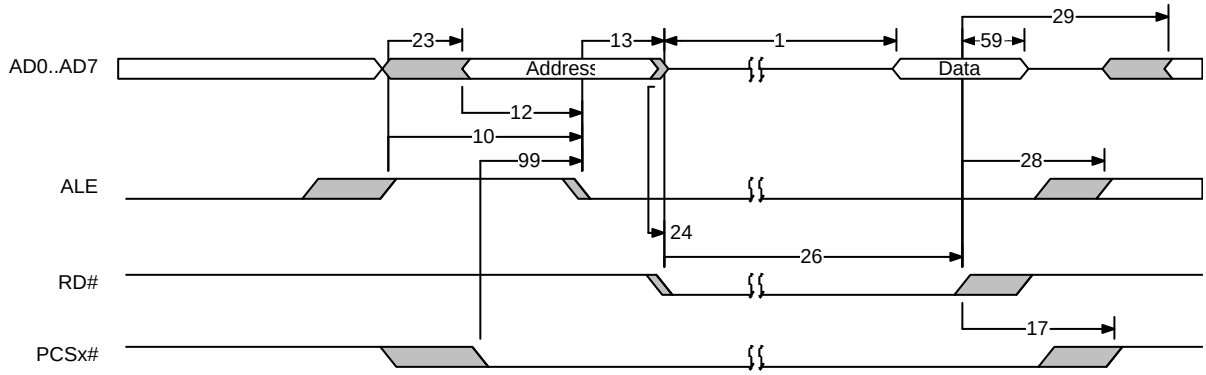
(Under operating ranges unless otherwise noted)

9.4.1 SC12-Read Cycle

T_A = 25°C

No.	Symbol	Description	Min	Max	Unit
General Timing Requirements					
1_a	t_{RLDV}	Read Valid to Data Valid (PCS0#..PCS3#)	65	65 + X[(1)]	ns
1_b	t_{RLDV}	Read Valid to Data Valid (PCS5#, PCS6#)	215		ns
59	t_{RHDX}	Read Inactive to Data Hold on AD Bus	0		ns
General Timing Responses					
10	t_{LHLL}	ALE Width	40		ns
12	t_{AVLL}	AD Address Valid to ALE Low	23		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive	23		ns
17	t_{CXCSX}	PCSx# Hold from Read Inactive	23		ns
23	t_{LHAV}	ALE High to Address Valid	20		ns
99	t_{PLAL}	PCSx# Active to ALE Inactive	15	28	ns
Read Cycle Timing Responses					
24	t_{AZRL}	AD Address Float to Read Active	0		ns
26_a	t_{RLRH}	Read Pulse Width (PCS0#..PCS3#)	85 + X[(1)]		ns
26_b	t_{RLRH}	Read Pulse Width (PCS5#, PCS6#)	235		ns
28	t_{RHLH}	Read Inactive to ALE High	22		ns
29	t_{RHAV}	Read Inactive to AD Address Active	40		ns

[(1)]X depends on wait states of PCS0#..PCS3# and can be 0..750ns (see @CHIP-RTOS Doc.)



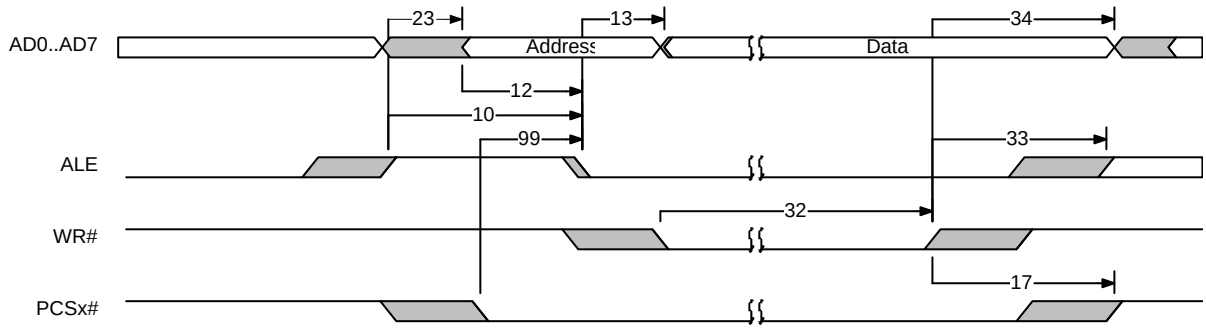
*) the falling edge of PCS0# is 50ns delayed internally

9.4.2 SC12 Write Cycle

T_A = 25°C

No.	Symbol	Description	Min	Max	Unit
General Timing Responses					
10	t_{LHLL}	ALE Width	40		ns
12	t_{AVLL}	AD Address Valid to ALE Low	23		ns
17	T_{CXCSX}	PCSx# Hold from Read Inactive	23		ns
23	T_{LHAV}	ALE High to Address Valid	20		ns
99	T_{PLAL}	PCSx# Active to ALE Inactive	15	28	ns
Write Cycle Timing Responses					
32_a	T_{WLWH}	Write Pulse Width (PCS0#..PCS3#)	90 + X[(1)]		ns
32_b	T_{WLWH}	Write Pulse Width (PCS5#, PCS6#)	240		ns
33	T_{WHLH}	Write Inactive to ALE High	23		ns
34	T_{WHDX}	Data Hold after Write Inactive	40		ns

(1)X depends on wait states of PCS0#..PCS3# and can be 0..750ns (see @CHIP-RTOS Doc.)



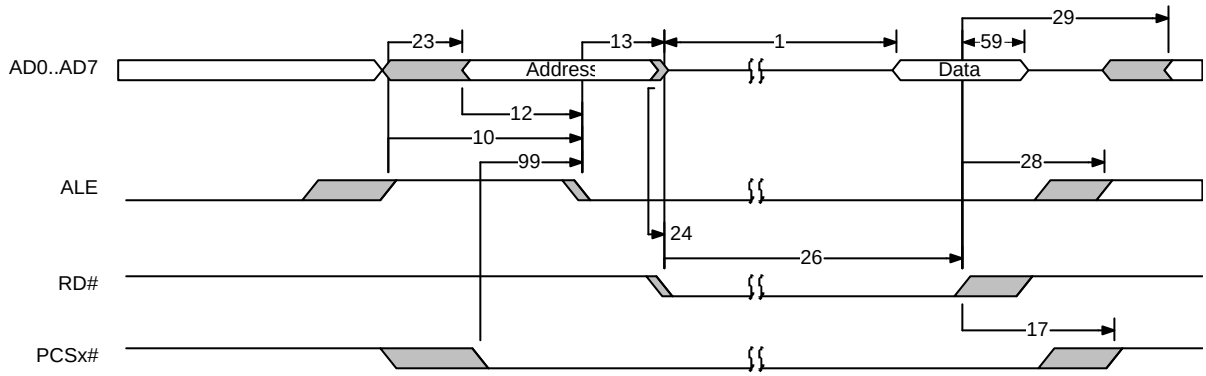
*) the falling edge of PCS0# is 50ns delayed internally

9.4.3 SC13/SC11 Read Cycle

T_A = 25°C

No.	Symbol	Description	Min	Max	Unit
General Timing Requirements					
1_a	t_{RLDV}	Read Valid to Data Valid (PCS0#..PCS3#)	12	12 + X[(1)]	ns
1_b	t_{RLDV}	Read Valid to Data Valid (PCS5#, PCS6#)	12	12 + X[(1)]	ns
59	t_{RHDX}	Read Inactive to Data Hold on AD Bus	0		ns
General Timing Responses					
10	t_{LHLL}	ALE Width	20		ns
12	t_{AVLL}	AD Address Valid to ALE Low	10		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive	10		ns
17	t_{CXCSX}	PCSx# Hold from Command Inactive	20		ns
23	t_{LHAV}	ALE High to Address Valid	10		ns
99	t_{PLAL}	PCSx# Active to ALE Inactive	23	30	ns
Read Cycle Timing Responses					
24	t_{AZRL}	AD Address Float to Read Active	0		ns
26_a	t_{RLRH}	Read Pulse Width (PCS0#..PCS3#)	20 + X[(1)]		ns
26_b	t_{RLRH}	Read Pulse Width (PCS5#, PCS6#)	20 + X[(1)]		ns
28	t_{RHLH}	Read Inactive to ALE High	10		ns
29	t_{RHAV}	Read Inactive to AD Address Active	20		ns

[(1)]X depends on wait states and can be 0.. 6375ns. (see @CHIP-RTOS Doc)



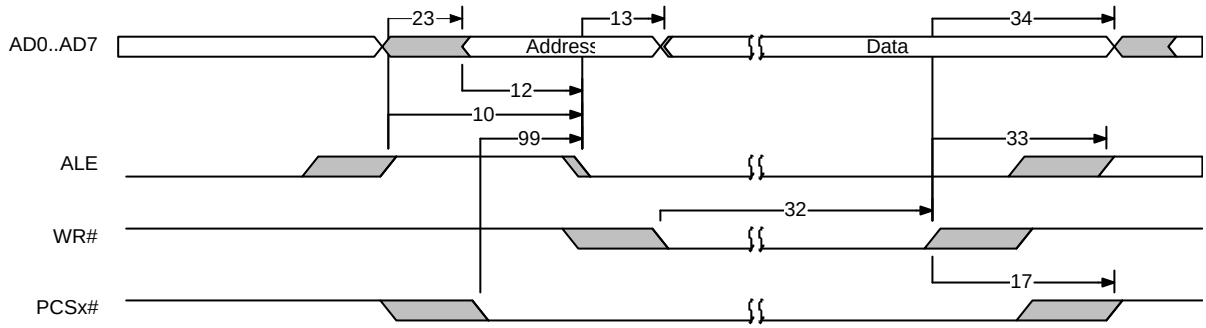
*) the falling edge of PCS0# is 25ns delayed internally

9.4.4 SC13/SC11 Write Cycle

T_A = 25°C

No.	Symbol	Description	Min	Max	Unit
General Timing Responses					
10	t_{LHLL}	ALE Width	20		ns
12	t_{AVLL}	AD Address Valid to ALE Low	10		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive	10		ns
17	t_{CXCSX}	PCSx# Hold from Command Inactive	20		ns
23	t_{LHAV}	ALE High to Address Valid	10		ns
99	t_{PLAL}	PCSx# Active to ALE Inactive	23	30	ns
Write Cycle Timing Responses					
32_a	T_{WLWH}	Write Pulse Width (PCS0#..PCS3#)	20 + X[(1)]		ns
32_b	T_{WLWH}	Write Pulse Width (PCS5#, PCS6#)	20 + X[(1)]		ns
33	T_{WHLH}	Write Inactive to ALE High	10		ns
34	T_{WHDX}	Data Hold after Write Inactive	15		ns

(1)X depends on waitstates and can be 0.. 6375ns. (see @CHIP-RTOS Doc)

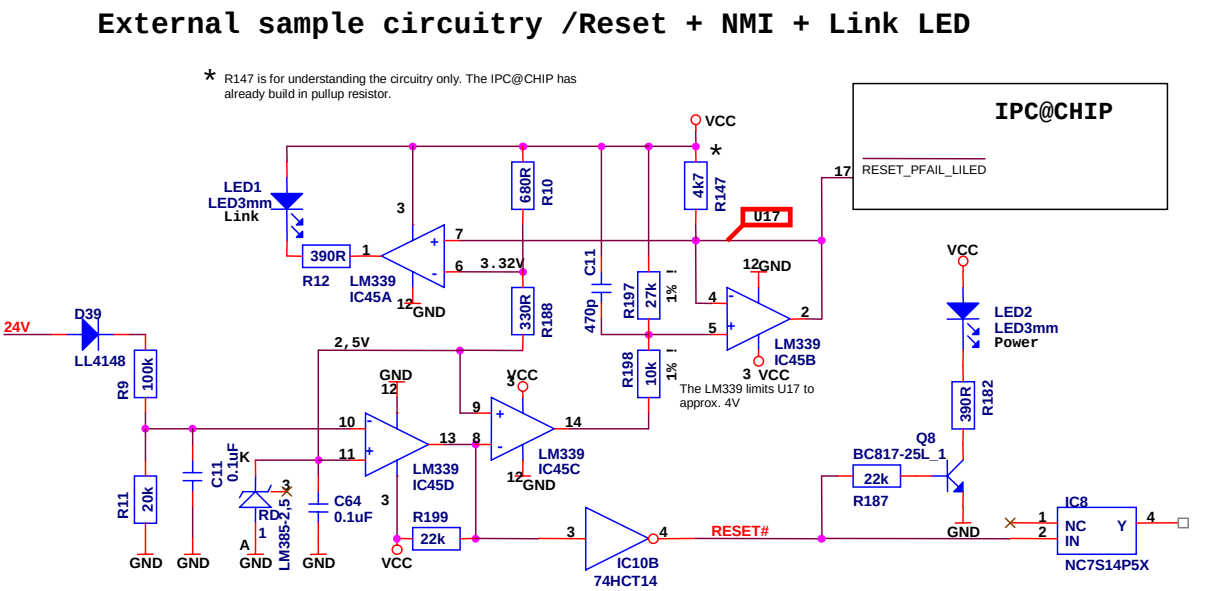


*) the falling edge of PCS0# is 25ns delayed internally

10. APPLICATION EXAMPLES

The following pages contain schematics showing the IPC@CHIP® family microcontroller. It gives you suggestions, how to handle the multi-function pin 17 RESET# / NMI / LINK-LED and how to expand the IPC@CHIP.

10.1 NMI / Reset-in / Link-LED



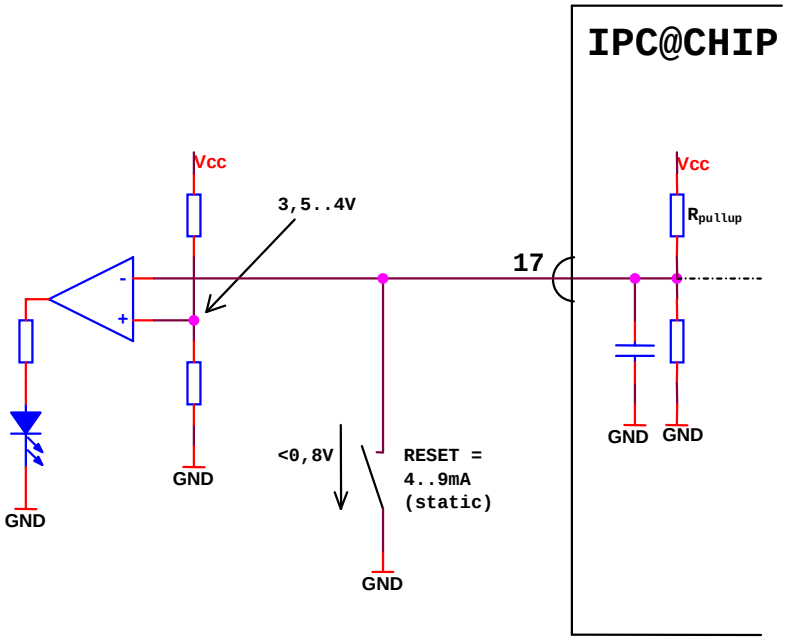
*) LM339 is an open collector operational amplifier

Picture 10.1: Example of using NMI, reset, traffic, (link[8]) at pin 17

See also DK50 schematic.

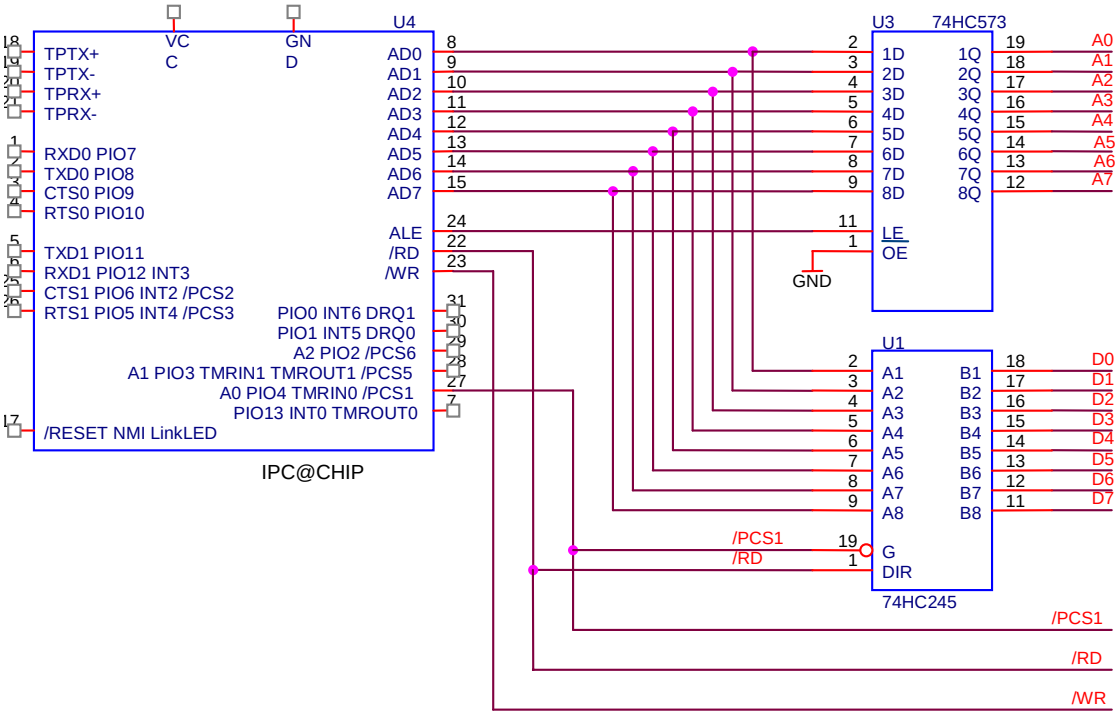
[8] only SC12

10.2 Link-LED / Reset



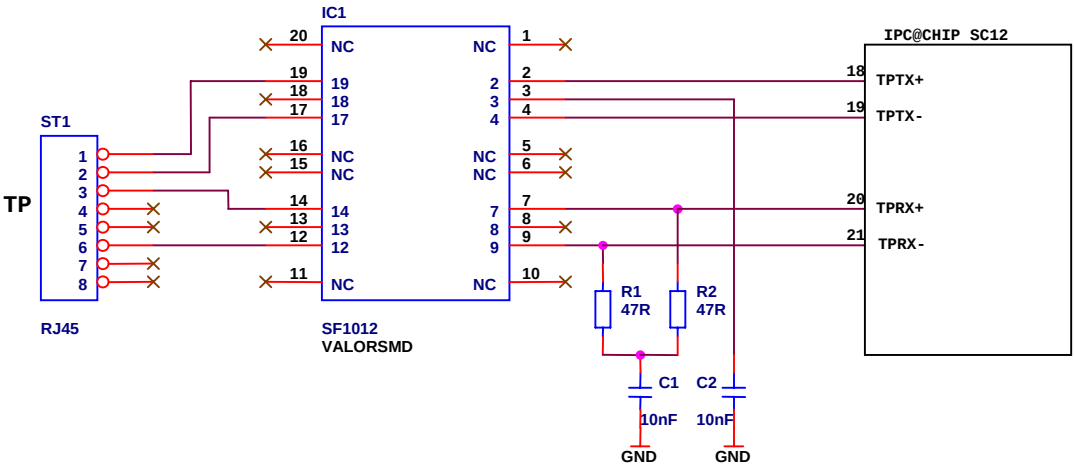
Picture 10.2: Link/traffic-LED / reset example

10.3 256x 8bit I/O Extension using 74HCT573/245

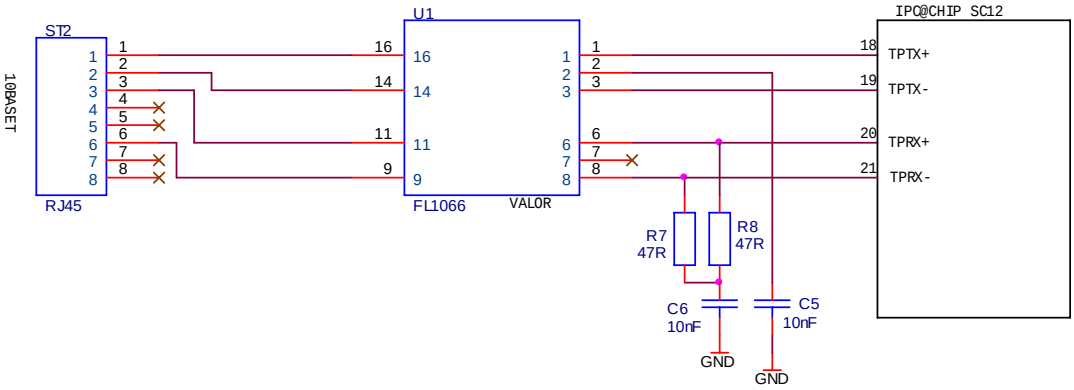


Picture 10.3: Example of a demultiplexed 8 bit A/D-Bus.

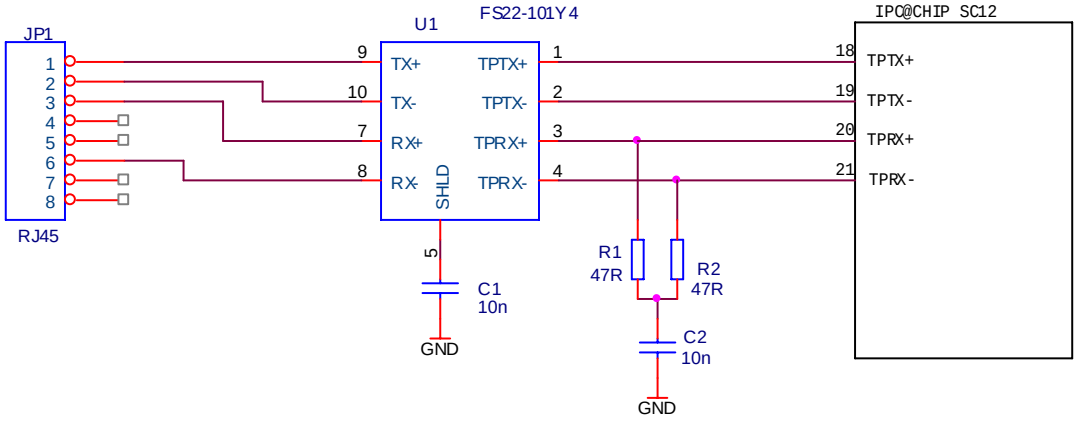
10.4 Connect 10Base-T Ethernet to the SC12



picture 10.4: Example of connecting 10Base-T to SC12 with SF1012

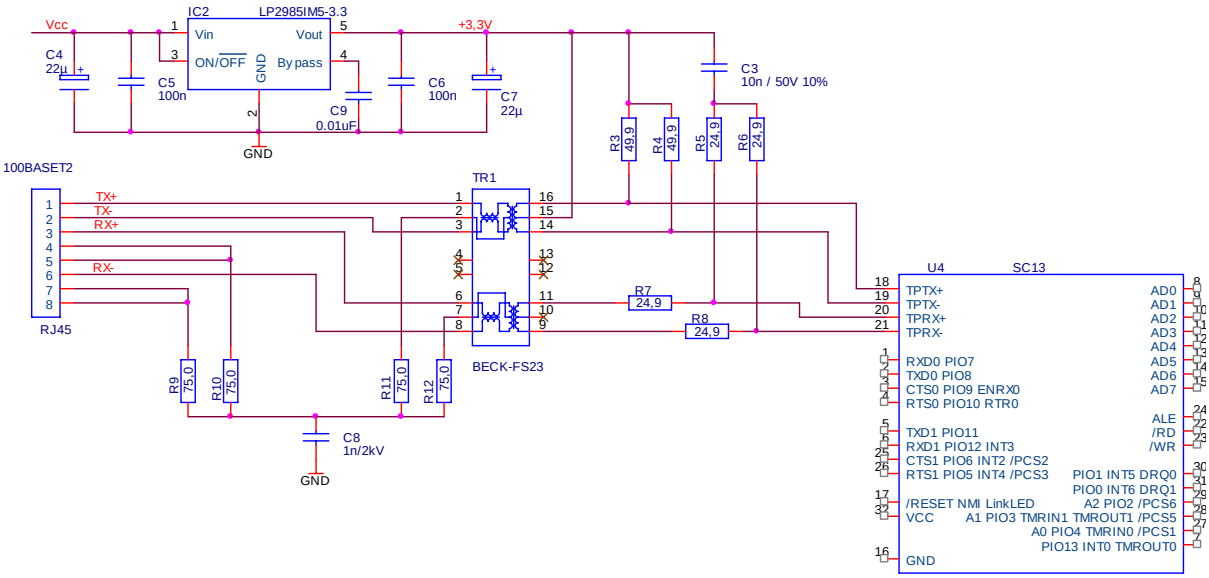


picture 10.5: Example of connecting 10Base-T to SC12 with FL1066

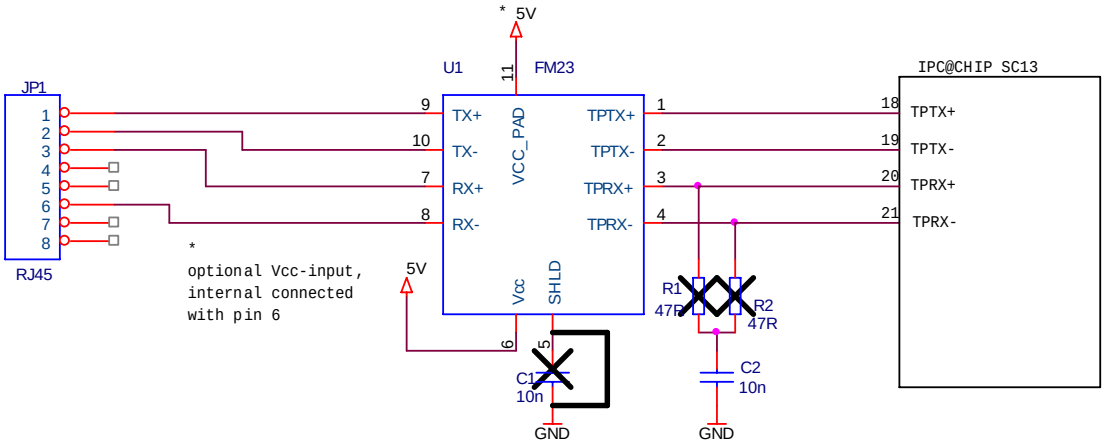


picture 10.6: Example of connecting 10Base-T to SC12 with FS22

10.5 Connect 10/100Base-T Ethernet to the SC13



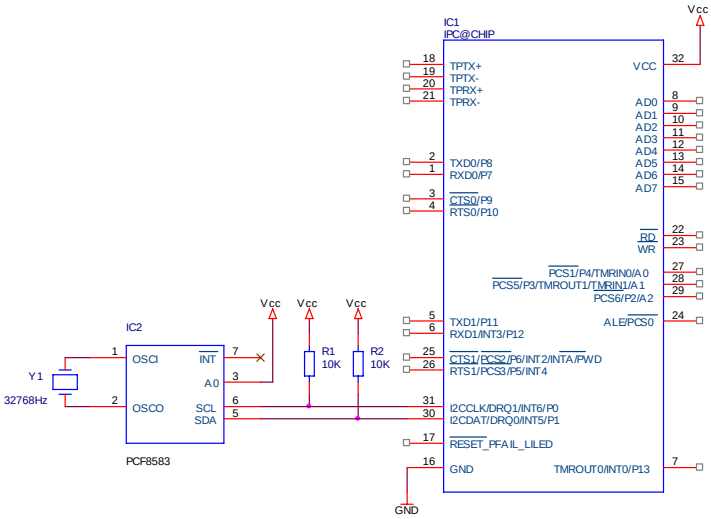
picture 10.7: Example of connecting 10/100Base-T to SC13 with FS23



picture 10.8: Example of connecting 10/100Base-T to SC13 with FM23
(convert SC12 schematic to fit SC13, see also picture 10.6)

10.6 I²C-Bus Example

To use PIO pins for I²C-Bus, connect a 10kΩ resistor to each PIO pin that is defined for I²C-Bus. The definition of initializing I²C-Bus is described in the @CHIP RTOS documentation.
The speed of the I²C-Bus is approximatly 40kHz max. for SC12 and 80kHz max. for SC13/SC11. A minimum speed can not be garanted, because it is a software emulation and depends hardly on the CPU load of the IPC@CHIP.



picture 10.9: Example of connecting a PCF8583 over I²C-Bus to the IPC@CHIP

10.7 SPI-Bus Example

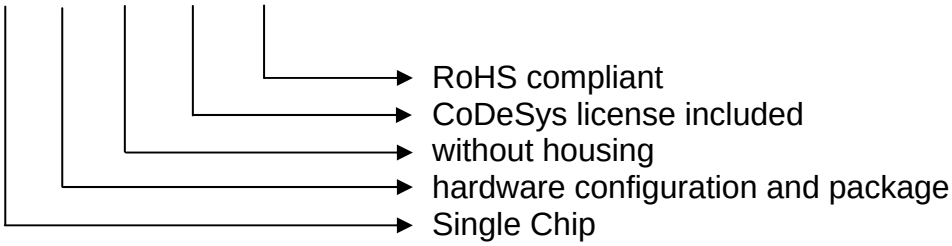
To use PIO pins for SPI-Bus, see SPI serial data flash example at Beck IPC Website and @CHIP RTOS documentation.

10.8 Other Examples

More examples are available at the download section of the Beck-IPC Website.

11. NOMENCLATURE

IPC@CHIP® **SC xxx** - **F** - **yyy** - **LF**



12. CHANGE LIST

Page 22
Changed Operating Temperature Range for SC11-LF and SC13-LF.

Page 9
Priciple schematic of pin 27 added.

Page 10
Priciple schematic of pin 24 added.

Page 20
Additional suggested magnetics.

13. CONTACT

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